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Studies of the Logical State of Integrated Microcircuits by Atomic Force Microscopy

A. M. Tagachenkov

Institute of Nanotechnologies in Microelectronics, Russian Academy of Sciences, Moscow 119991, Russia
e-mail: alexmitag@yandex.ru

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Abstract—The logical state of the memory cells in a nondestructive microcontroller was determined and analyzed by atomic-force microscopy. An effective optimal recording procedure of the electric potential on the microchip surface was created.

Key words: atomic force microscopy, study of integrated circuits.

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INTRODUCTION

This work was aimed at revealing the possibilities of modern nondestructive diagnostic facilities for microcircuit crystals and testing methods for the reconstruction of lost information. To locally analyze the distribution of the electric potential on metal, dielectric, and semiconductor nanostructured crystal layers of very-large-scale integration (VLSI) schemes, electrostatic force microscopy (EFM) and Kelvin probe force microscopy (KPFM), which are varieties of atomic-force microscopy (ASM) [1–3], are of practical interest.

Studies on the recording and identification of the logical state of memory cells of integrated microcircuits (IMC) were performed using these methods by the example of single-crystal Pic16F84A microcontroller (MicroChip Technology) [4] without the removal of passivating coatings while keeping the functionality of the product. An effective optimal recording procedure of the electric potential on the IMC surface was created.

1. METHODS

To control the electric potential on the VLSI crystal surface, a hardware–software complex on the basis of AFM was used. This research complex contains a measuring block created on the basis of a Solver P47H atomic-force microscope (NT-MDT, Zelenograd) and a block recording the logical signal supplied on the studied device consisting of a generator and an analyzer of the logical signal (Laboratory of Automated Systems, Moscow).

To adjust the necessary measurement modes of the hardware–software complex and to study the spatial and time resolution, and to determine the sensitivity of the measurements of the surface electric potential in EFM and KPFM modes, $Si/SiO_2/Ti$, Si/Ti, and $Si/Al/SiO_2$ test structures were designed, produced, and applied. It was established, in particular, that the sensitivity of the measurements was not worse than 100 mV in atmospheric conditions and that the locality upon functioning in the KPFM mode was about 50 nm.

The studied Picl6F84A microcircuit is a single-crystal microcontroller produced using complementary metal–oxide–semiconductor (CMOS) technology. It contains three memory regions: electrically erasable programmable read-only memory (EEPROM) of the flash memory type (FLASH), mask memory of the read-only memory device (ROM) and memory of the random access memory device (RAM). To study the logical state of the memory cells of a crystal, the EEPROM memory of the FLASH type is of the highest interest.

The electric potential was measured on the surface protective insulation coating of Picl6F84A for three schemes of IMC connection:

(1) Upon connection of the IMC to a programmer and constant addressing of the crystal memory;

(2) Upon connection of the IMC to a power source of +5 A, with the information being recorded preliminarily in a crystal by means of a programmer;

(3) With the IMC power supply switched off with the information being recorded preliminarily in the crystal by means of a programmer and grounded wires.

2. RESULTS AND DISCUSSION

First of all, the logical state of the memory cells of the Picl6F84A microcircuit was studied for the first scheme of IMC connection, where the crystal memory region is permanently addressed (the trigger voltage is supplied to the address bus) and the cell transis-

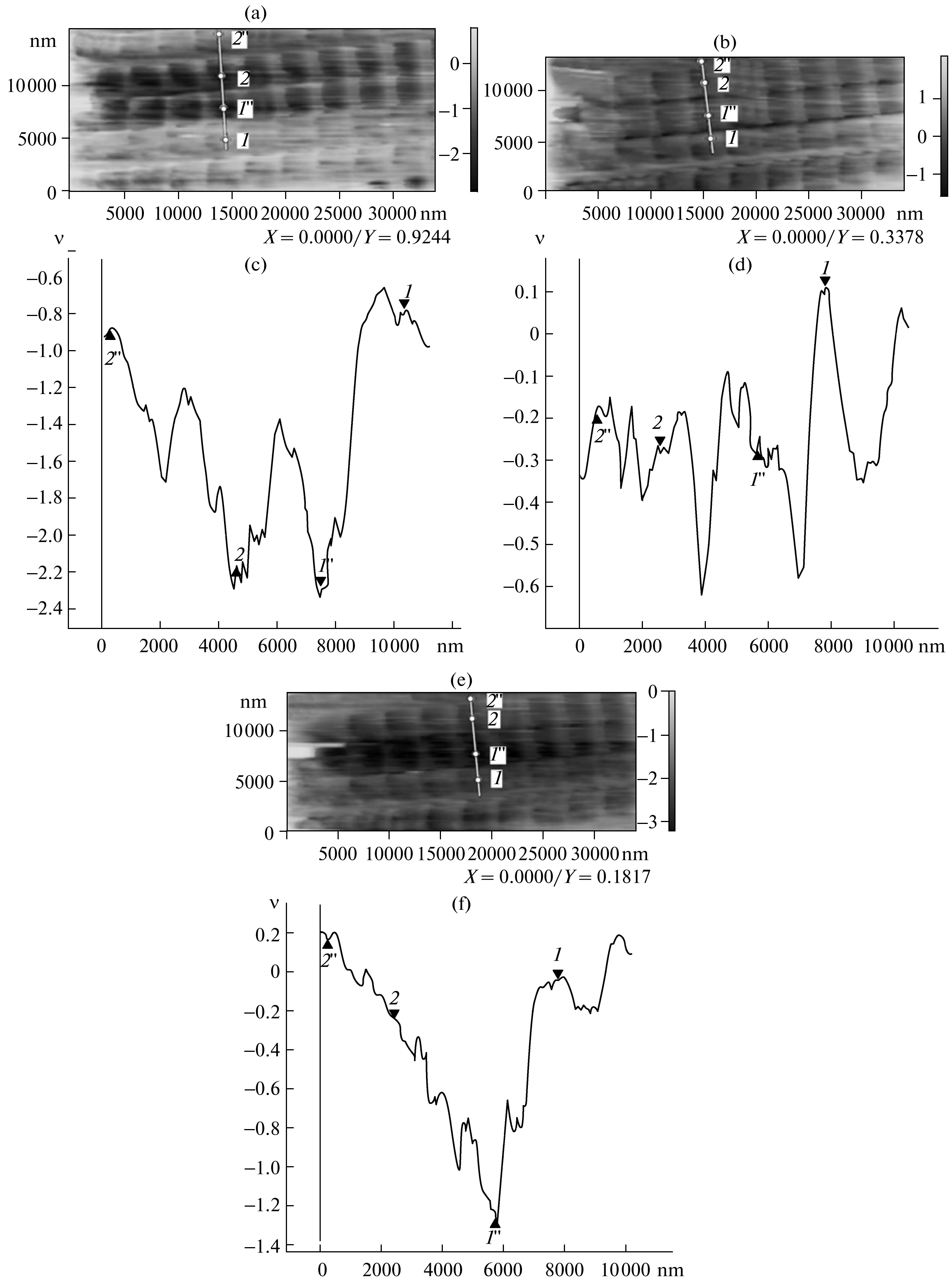

Fig. 1. AFM images (KPFM mode)) of a fragment of the crystal surface upon recording: “FF” (a), “0” (b) and “55” (e) and the corresponding distribution diagrams of the electric potential along the specified lines. Scan size, 10 × 10 μm.

tor is connected to the discharge bus. As a result of the fact that the clock frequency of the pulse programmer does not coincide with the sweep frequency of the AFM frame, longitudinal noise is observed in the potential contrast image. Figure 1 shows an AFM image of the fragment of the crystal surface in the KPFM mode when information is recorded in the binary code of hexadecimal calculus: (a) "FF," (b) "0," (e) "55" and the corresponding distribution diagrams of the electric potential along the specified lines. One can see that the potential difference between logical states "FF" and "0" is about 2 V (Figs. 1c and 1d). Figure 1f shows that the potential difference between similar levels was about 1 V. This can be explained by the close location of the floating shutters of the cell transistor and the superposition of contrasts due to the different charge states in the neighboring memory cells.

The studies of the logical state of the memory cells of the microcontroller when using the second scheme of crystal connection showed that upon measuring the electric potential at the peripheries of the memory field and functional regions under potential, noise due to the fact IMC wires can occur, unless the power supply and ground are in the unplugged state. If the power supply is unplugged, the noise disappears. Upon measuring the electric potential inside the homogeneously recorded memory field, screening of the useful signal due to the inhomogeneities of the surface state of the dielectric and unplugged IMC wires can be observed. These studies allowed us to establish that without the power supply the range of the changes of the potential difference between the opposite logical states 0 and 1 is strongly narrowed (by two times) when compared with the measurements with the power source switched on. The bottom boundary of the potential difference is higher by 0.15 V, which it is important for the identification of IMC logical states.

Upon studying the logical state of the memory cells of the microcontroller when using the third scheme of the crystal connection it was revealed that the process of the polarization of the upper dielectric is time consuming and reaches 20–30 min.

The constructive analysis of the structure of the cell memories of the microcontroller allowed us to determine that the floating shutters of the control transistor are in the direct vicinity of each other; therefore, analysis of the electric potential on the surface of the upper dielectric layer after recording information about the opposite logical state in the neighboring cells is of the most interest. It was shown that a twofold increase in the time of the polarization of the upper dielectric layer occurs, of 40–60 min. These observations indicate that at the moment of recording the studied state the processes of recombination and transfer of the charge carriers in the crystal structure are not finished.

CONCLUSIONS

Effective engineering solutions and methods providing high-spatial-resolution nondestructive control of the functioning of EEPROM memory cells of the FLASH type by means of atomic-force microscopy were created.

The logical state of the memory cells of integrated Picl6Fb4A microcircuits was studied without removing their passivating coatings and while retaining the functionality of the products. The optimal methods for recording the electric potential on the IMC surface were specified.

The variant with the power supply of the IMC switched off and preliminary recording of information in the crystal by means of the programmer and grounded wires turned out to be the most efficient one of the three different schemes of microcircuit connection.

These results showed that it is possible to use the methods of scanning force microscopy for the nondestructive diagnostics of processes and analysis of logical signals in element electronic devices. The use of similar methods allows one to perform not only the nondestructive diagnostics of electronic systems, but also to determine the presence of subsurface localized charges with high resolution and to perform subsurface nanotomography of the charge states and electric potentials.

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